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# PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS EVALUATION BOARD OPERATING GUIDE



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# PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS EVALUATION BOARD OPERATING GUIDE



## 1.0 Applicable Products

HMC767LP6CE, HMC769LP6CE, HMC778LP6CE

## 2.0 Introduction

This Operating Guide covers the specified family of Hittite fractional synthesizer with integrated VCO. Section 3 lists the evaluation Kit contents. Sections 4 and 5 describe how to operate the evaluation board.

## 3.0 Evaluation Kit

The evaluation kit contains the following contents:

a. (1) Evaluation Board Part #:
130369-HMC767LP6CE or 130370-HMC769LP6CE or 130371-HMC778LP6CE

b. (1) CD ROM Part # 121325

c. (1) USB Controller Board # 122046

d. (1) USB Cable # 690-00064-00

e. (1) Control Cable # 595-00199-00

The CD ROM should include the followings files as a minimum:

a. FTDI USB Drivers .zip file

b. VB HMC Synthesizer Controller Software

c. PLL Design Software

d. Recommended PLL Register Set Text File

e. README Installation Guide

## 4.0 Evaluation Board Operation

### 4.1 Configuration with On-Board Crystal Oscillator

The evaluation board of Hittite fractional synthesizer with integrated VCO should be set up as shown in the Figure 1. It should be noted that very low noise synthesizers are sensitive to noisy power supplies. The evaluation board provides on-board regulators to isolate the +5.5V supply from the PLL analog and digital +3.3V supplies, the PLL Charge Pump +5V supply and the VCO +5V supply. The VCXO is also regulated separately to +3.3V from the +5.5V external supply.

The very low noise of the synthesizer requires a high quality test instrument to observe the phase noise or jitter. For this we recommend a signal analyzer such as the Agilent E5052B or equivalent. A high performance spectrum analyzer can be used as an alternative to the signal analyzer.

Figure 2 highlights the major components and connectors on the Synthesizer evaluation Board.

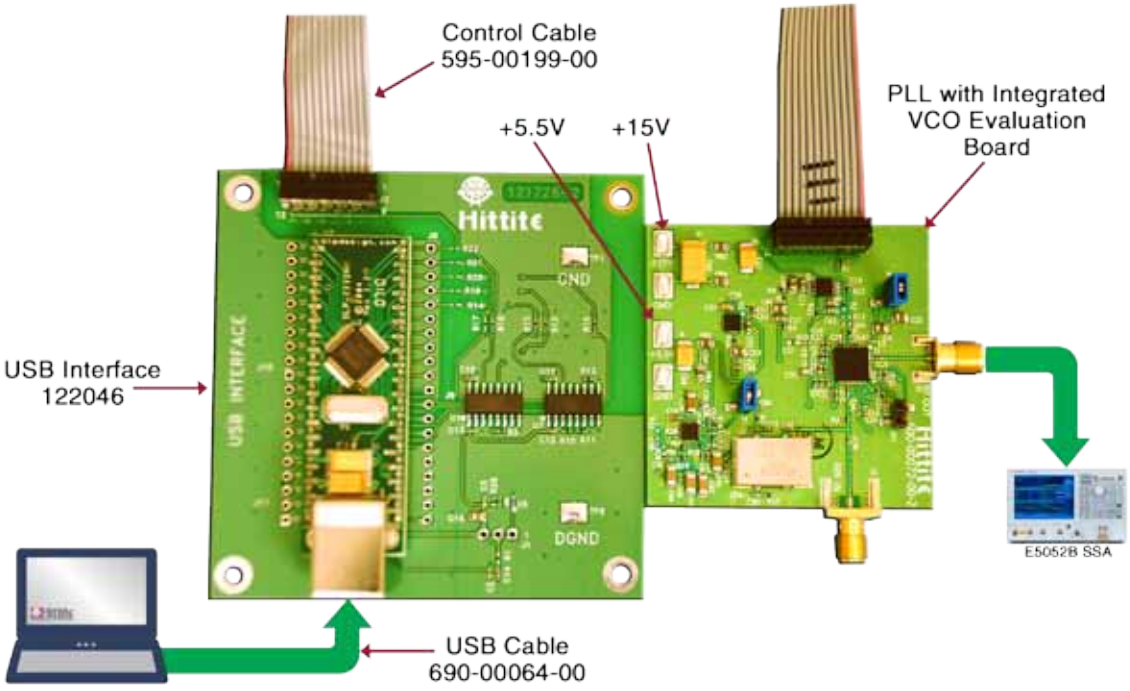


*Figure 1. Typical Setup of Synthesizer evaluation Board*

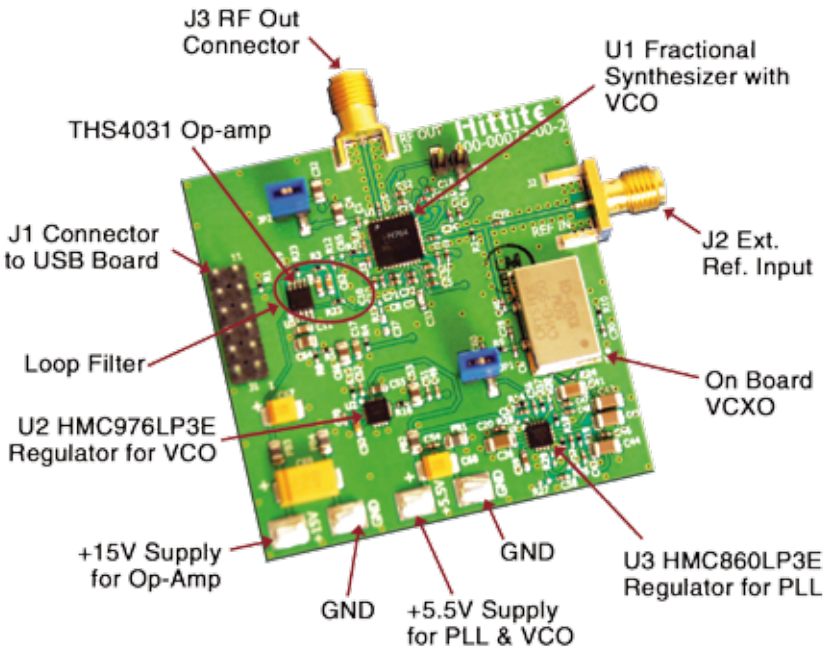


*Figure 2. Synthesizer Evaluation Board Major Components*

## 4.2 Configuration with External Crystal Oscillator

If it is desired to use the evaluation board with an external crystal oscillator, disconnect the VCXO power supply by leaving JP1 open, and connect the external source to J2 as shown in Figure 3. If the external source has sufficient drive (see the reference sensitivity plots in datasheets) it is likely not necessary to remove C34, at the output of the on-board crystal oscillator, otherwise remove C34 from the board. The evaluation board has been tested with an external 100MHz sine crystal with C34 in place with no measurable effects, however an external square wave oscillator may be more sensitive to mismatch caused by C34, hence if in doubt, remove C34.

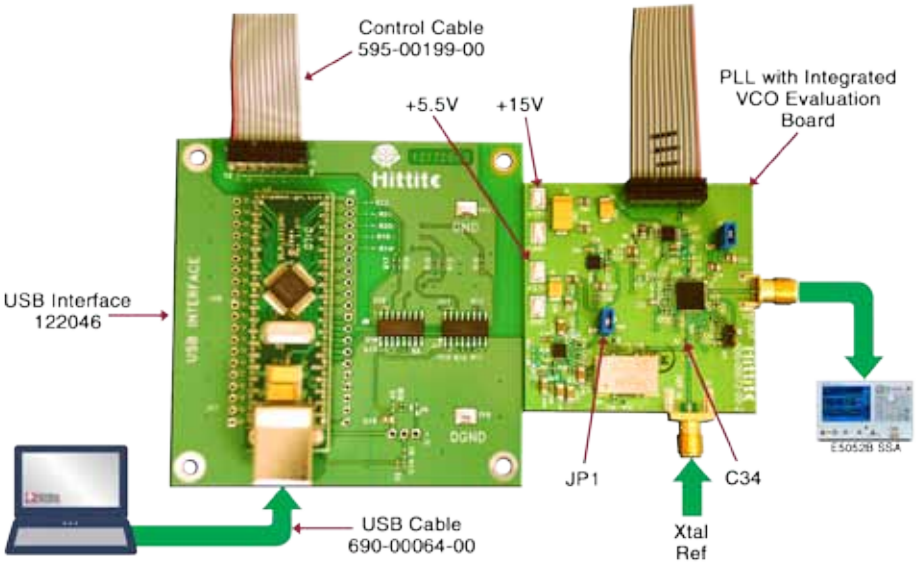


*Figure 3. Typical Setup of the Synthesizer Evaluation Board with External Crystal Oscillator*

## 4.3 Configuration with the Different Types of Loop Filters

### 4.3.1 General Schematic Of Loop Filter

Depending on the user requirements, some type of loop filters can be configured on the evaluation board. A general schematic of loop filters is shown in Figure 4. It can be configured into Passive filter or ActiveC filter. It should be noted that the default loop filter on the evaluation board is ActiveC. R23 is set to zero ohm, while C65 is open as it is optional. R23 and C65 can be configured for a higher order filter to improve the spur performance.

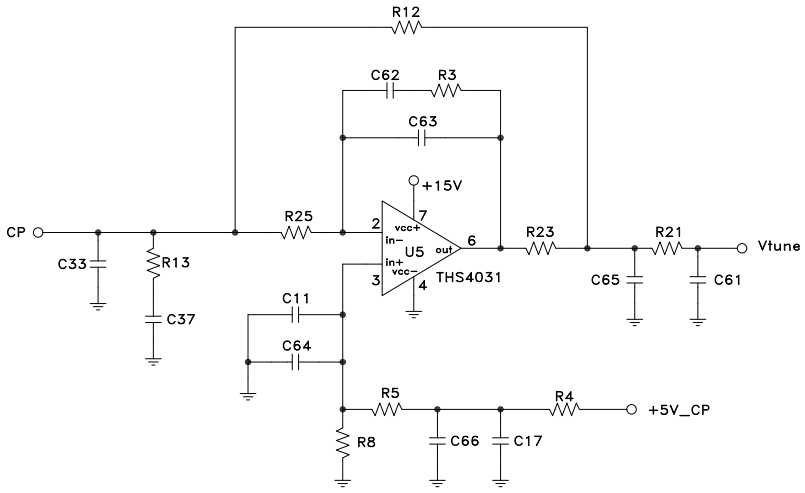


*Figure 4. General Schematic of Loop Filter*

### 4.3.2 Passive Loop Filter

Based on the general schematic above, some type of loop filters can be configured as follows.

It should be noted that the Op-amp is powered by a separate power supply, marked +15V.

a. Passive Loop Filter

The Passive loop filter consists of C33, R13, C37, R21 and C61. It can be configured by removing R4, R23, R25, C65, shorting R12=0, and leaving +15V open.

It should be noted that the maximum VCO tuning voltage of the passive loop filter is limited by the charge pump power supply, for example, +5V.

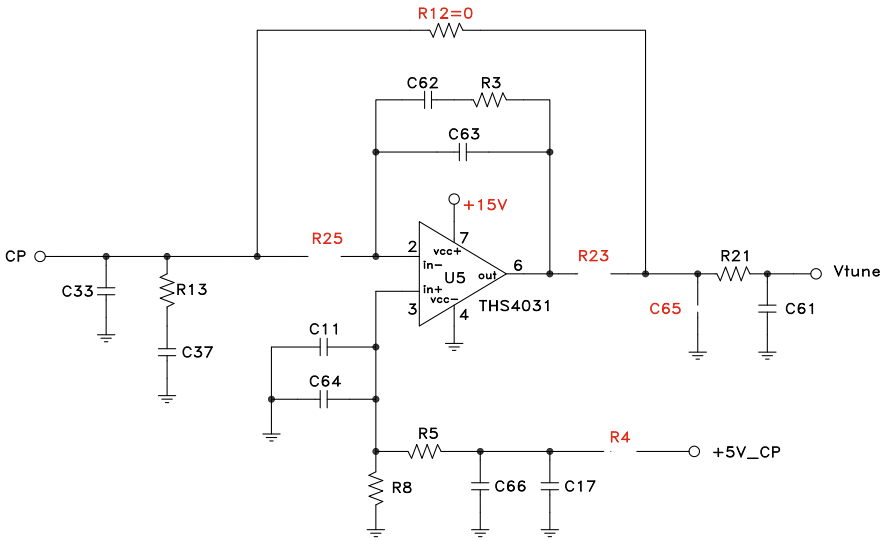


*Figure 5. Passive Loop Filter*

### 4.3.3 ActiveC Loop Filter

The ActiveC loop filter consists of C33, R25, C62, C63, R3, R21, C61, R5, R8, C11, C17, C64, C66 and Op-amp U5. It can be configured by removing R12, R13, C37, C65, shorting R4, R23, and powering +15V on.

It should be noted that the ActiveC loop filter is a very popular choice since it does not have the maximum Vtune limit as the Passive loop filter does.

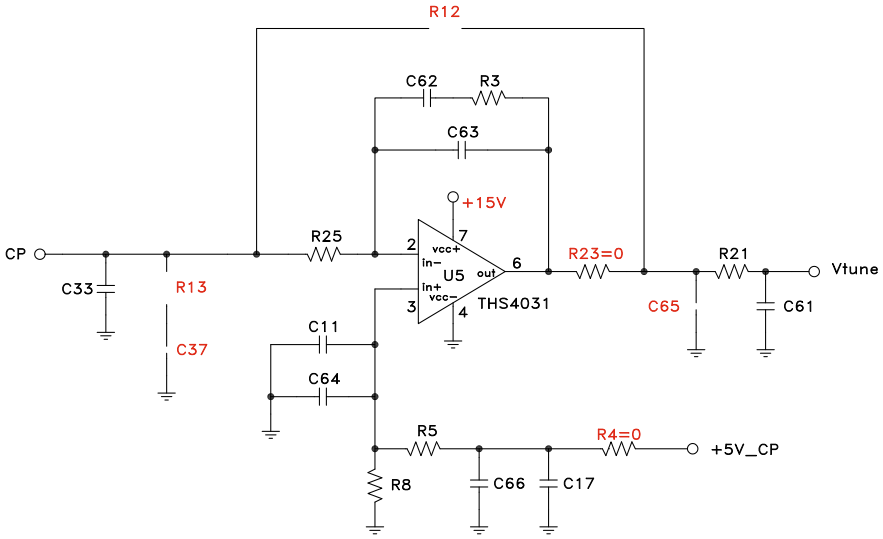


*Figure 6. ActiveC Loop Filter*

## 5.0 Operating Procedure

**Step 1.** Setup the evaluation board as shown in Figure 1

**Step 2.** Turn +5.5V and +15V supplies on.

**Step 3.** Launch the control program (located initial on the CD).

**Step 4.** From the drop down list, select the part you are operating (for example, HMC778LP6CE).


*Figure 7. Part Selection Menu*

**Step 5.** Click “Done” button, the main control window pops out as Figure 8 shown.

**Step 6.** Click “Load Reg File” button to load the register contents of the part (Figure 9.)

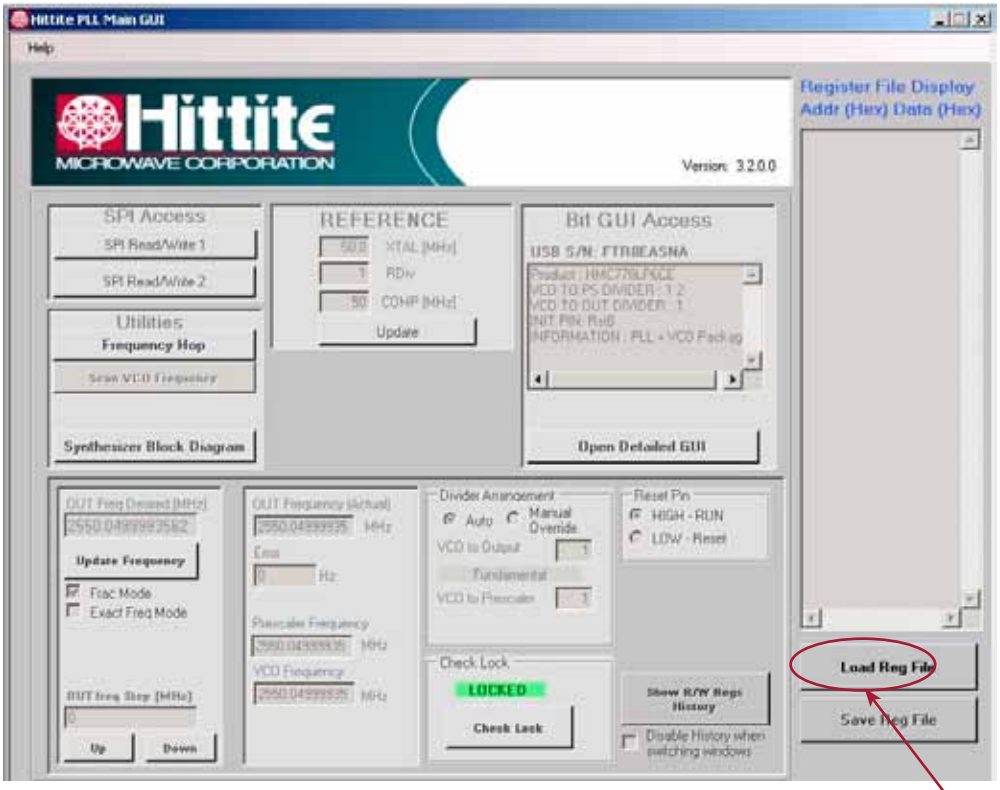


*Figure 8. Main Control Window*

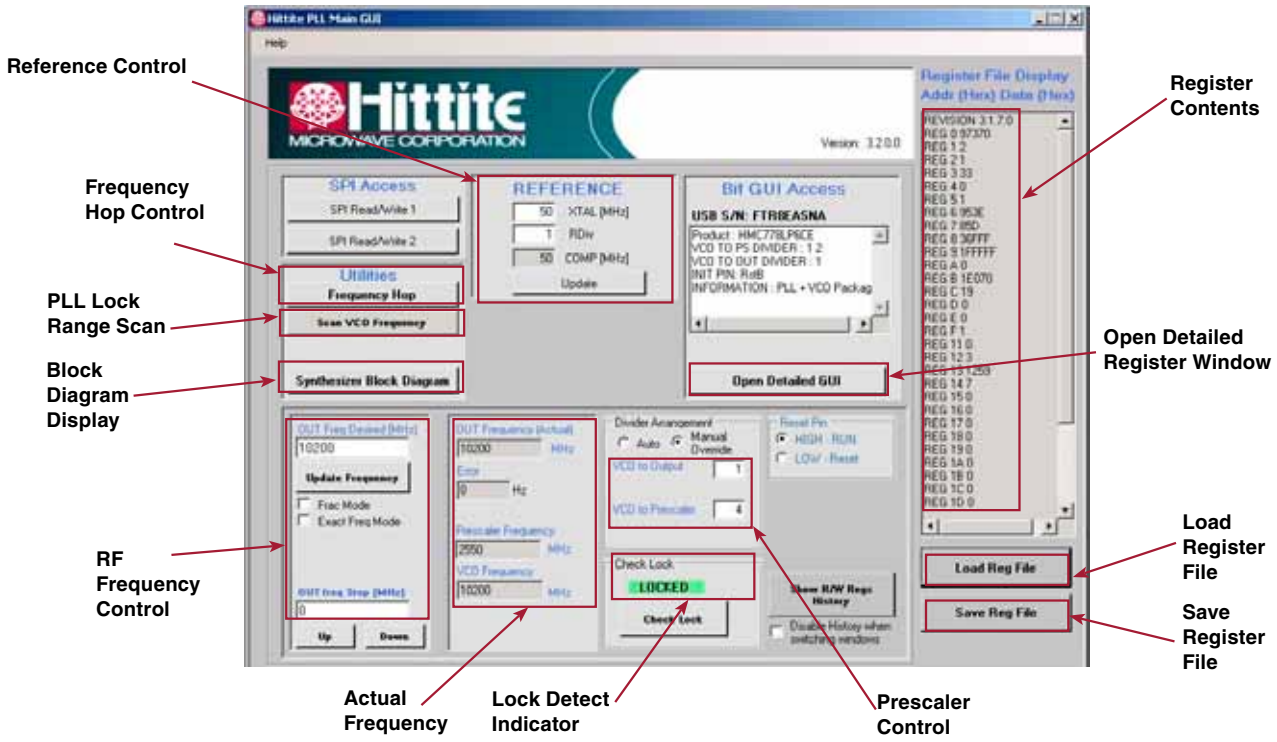


*Figure 9. Main Control Window After Loading Register File*

**Step 7.** Click "HMC Synthesizer Block Diagram" button, the block diagram pops out as Figure 10 shown (optional to show the configuration but step not required to run the part).

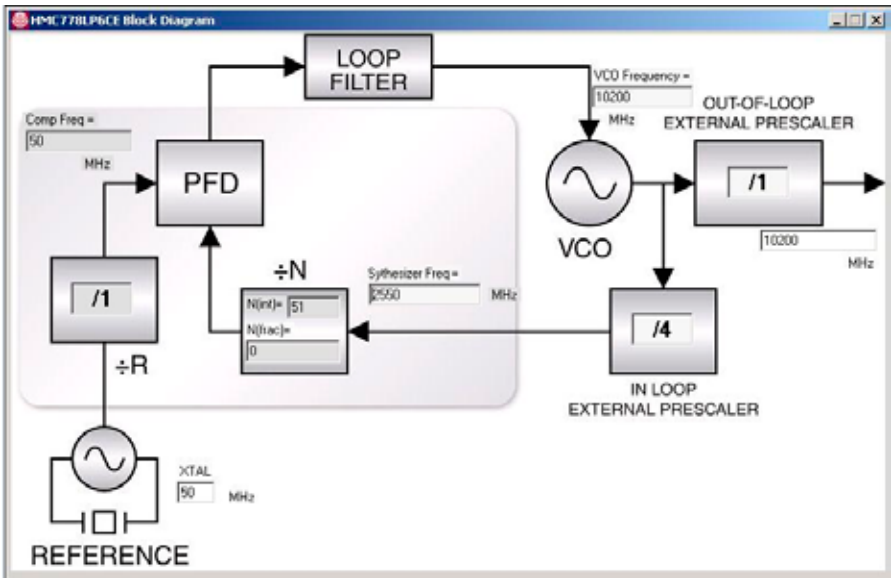


*Figure 10. Synthesizer Block Diagram*

**Step 8.** Set RF frequency in “RF Frequency Control” block.

Check “Manual Override” and change “VCO to Prescaler” from “1” to “4” in Prescaler Control block. For integer mode, type in the frequency desired, click “Update Frequency” button as Figure 11 shown. User can click “Open Detailed GUI” button to see the detailed register window in integer mode as shown in figure 12.

For fractional mode, check “Frac Mode” box first. Then type in the frequency desired, click “Update Frequency” button as Figure 13 shown. In order to optimize the phase noise and spur performances in fractional mode, user should click “Open Detailed GUI” button. The new detailed register control window pops out as shown in Figure 14. In the “Register 09: Charge Pump Register” block, check “Source CP Offset” box or “Sink CP Offset” box and select the calculated CP offset current from the pull down list of “CP Offset” box. Then click “write” button. The correct CP offset current is calculated by the following equation (see Equation 4 on page 19 of HMC703LP4E datasheet).

Required CP Offset Current = (2.5*10E-9 + 4*Tps)*Fcomp*Icp

Usually this value will give the optimum performances on phase noise and spurs.


*Figure 11. Main Control Window in Integer Mode*

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**For the integer mode, these three boxes are unchecked.**

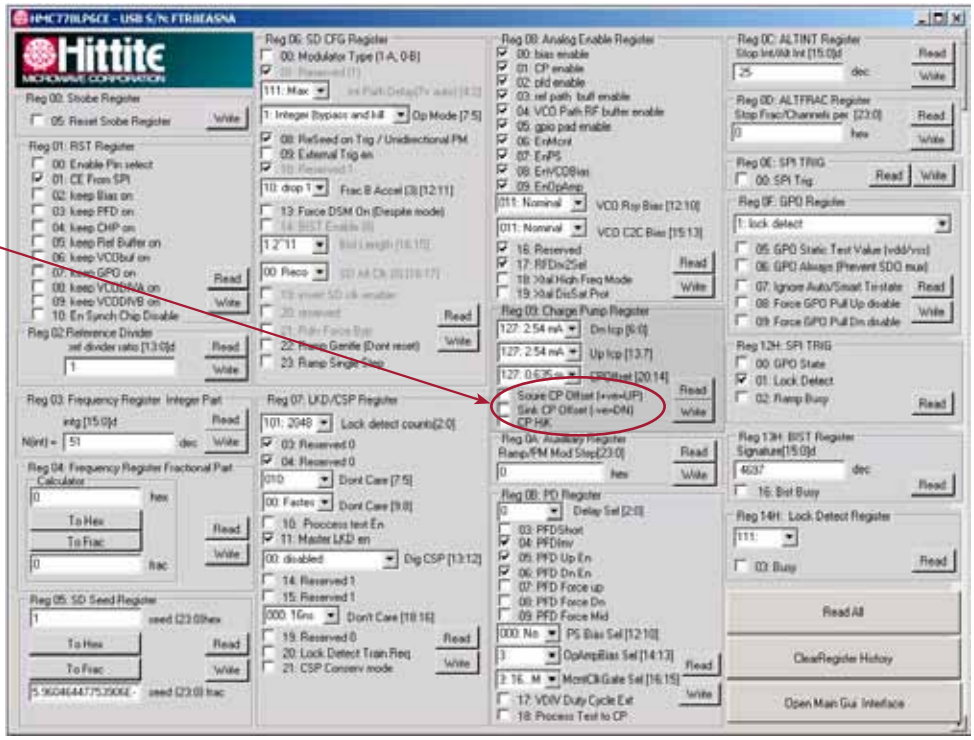

*Figure 12. Detailed Register Window In Integer Mode*

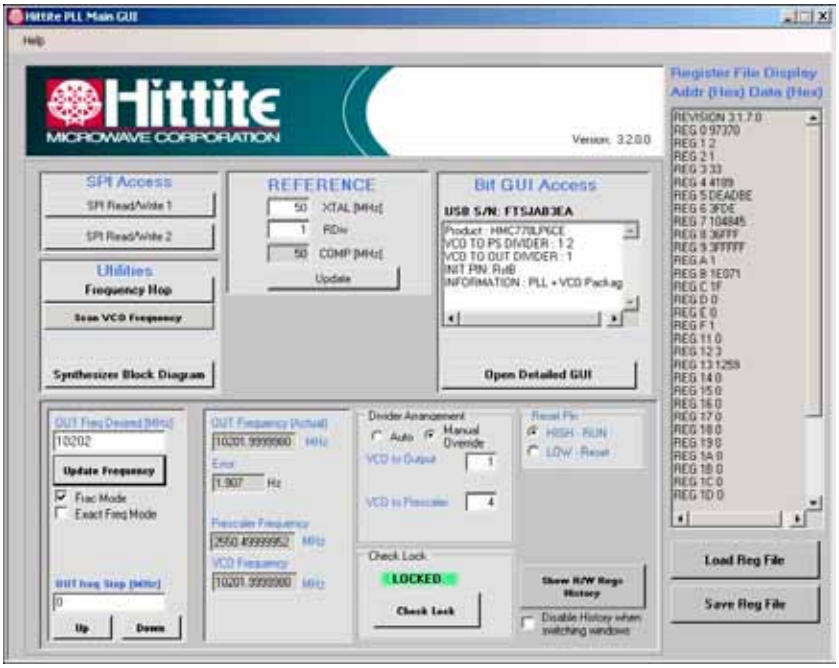

*Figure 13. Main Control Window in Fractional Mode*

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**For fractional mode, "Sink CP Offset" or "Source CP Offset" box should be checked and the calculated offset current should be selected from the pull down list of "CP Offset" box.**

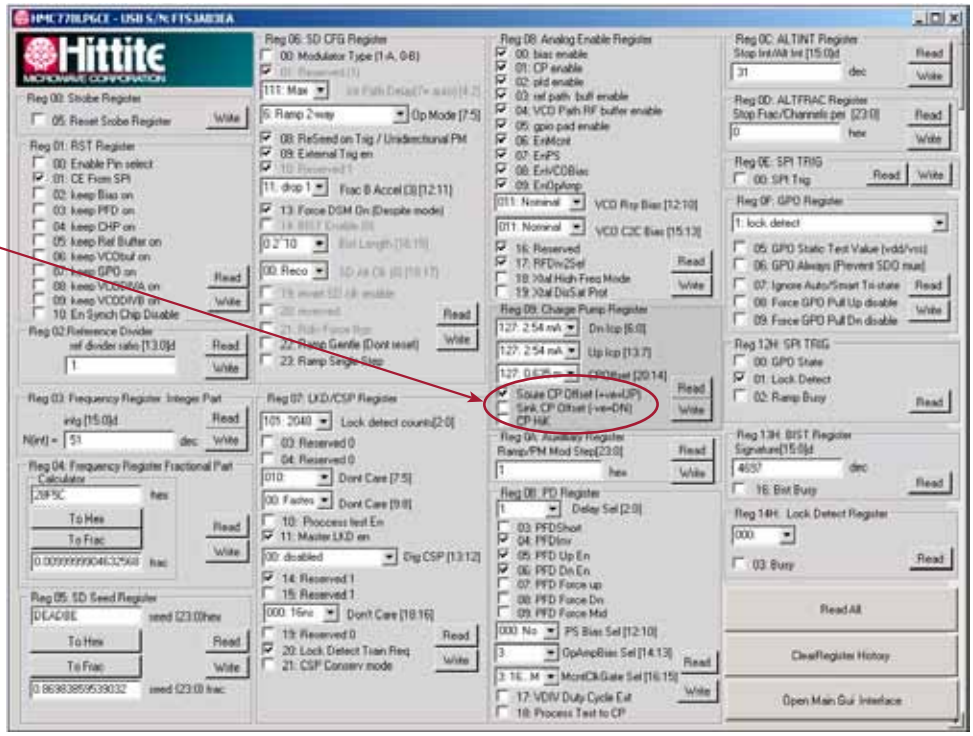

*Figure 14. Detailed Register Window In Fractional Mode*

**Step 9.** Scan the VCO frequency to find the synthesizer locked range ("Frac Mode" box must be checked).

Click "Scan VCO Frequency" button in the main control window (Figure 9). A new small window pops out as shown in Figure 15. Set "Start Freq", "Coarse Step" and " Freq Max Limit", click "Start Scan" button (refer to the specified Min/Max frequencies of the particular part in the datasheet, set "Start Freq" to Min frequency and set "Freq Max Limit" to 1 GHz above Max frequency). When the scan is finished, the synthesizer locked range will be shown in the window. As an example, Figure 16 shows the scan setting and scan result on HMC778LP6CE. Remember that the frequency lock range is greater than the specified frequency range and the phase noise or spurs will degrade outside of this specified window.

**Step 10.** Run frequency hopping (optional).

Click "Frequency Hop" button in the main control panel (Figure 9). A new small window pops out as shown in Figure 17. Set "Frequency #1", "Frequency #2" and "Dwell Time" in this window. Then click "Start" button. The RF signal will switch between "Frequency #1" and "Frequency #2" in the defined "Dwell Time". Figure 18 shows a typical example of the "Frequency Hop" setting on the HMC778LP6CE. This function usually is used to find the frequency settling time of the synthesizer.

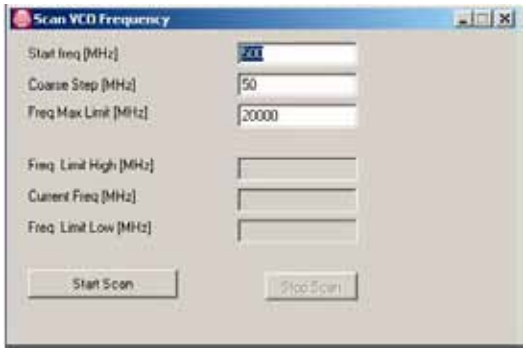


*Figure 15. Default "Scan VCO Frequency" Window*


*Figure 16. Scan Setting and Scan Result on HMC778LP6CE*


*Figure 17.Default "Frequency Hop" Window*


*Figure 18.Typical Setting Example of FrequencyHop*